## REMARKS

This is in full and timely response to the non-final Office Action mailed on June 17, 2002. Reexamination in light of the amendments and the following remarks is respectfully requested.

Claims 1-3, 5-7, 10-42 are currently pending in this application, with claims 1, 3 and 25 being independent.

No new matter has been added.

**Drawings**

The Office Action indicates that the drawing corrections of February 27, 2002 have been approved while also indicating that proper drawing corrections are required to avoid abandonment.

This indication lacks clarity since drawing corrections have been provided and approved. Clarification is respectfully requested.

**Rejection Under 35 U.S.C. §112**

Claims 38 were rejected under 35 U.S.C. 112, second paragraph.

Claim 38 was rejected for having a lack of an antecedent

basis for the term "said time-division switch."

In response, while not conceding the propriety of this rejection and in order to advance prosecution, claim 38 has been amended. Withdrawal of this rejection is respectfully requested.

**Rejection Under 35 U.S.C. §102**

Claims 1-12 and 17-39 were rejected under 35 U.S.C. 102 as allegedly being anticipated by U.S. Patent 4,825,203 issued to Takeda et al. (Takeda).

This rejection is respectfully traversed for at least the following reasons.

Figure 1 and page 2, lines 12-20 of the specification as originally filed describe a conventional example where general driver ICs 101 are used. In this conventional example, each general driver IC 101 has the same number of outputs. But only some of the total number of outputs for one of the general driver IC is used while there are a remaining number of outputs of a general driver IC that are unused.

Conversely, claim 1 and claims dependent thereon provide that if a fraction occurs in the signal lines of the plurality of

columns, the number of output terminals of one of the plurality of driver circuits is set to the fraction.

In this regard, page 13, lines 18-26 of the specification as originally filed describes a novel example where general driver ICs 14 are used along with a remainder driver IC. Each one of the general driver ICs 14 has the same number of possible total outputs as another of the general driver IC 14 and all of the possible total outputs are used. The remainder driver IC has a possible total outputs that is different than the possible total outputs of any of the general driver ICs 14 and all of the possible total outputs of the remainder driver IC are used.

Figure 2 of Takaeda arguably teaches a plurality of signal lines 11-b (column 2, line 63) and a driver circuit 13. Figures 1(A) and 1(B) arguably depict the details of the driver circuit 13 having a plurality of buffers 36 connected to the signal lines (column 5, lines 4-5). However, Takaeda fails to teach that <u>if a fraction occurs in the signal lines of the plurality of columns, the number of output terminals of one of the plurality of driver circuits is set to the fraction</u>, as claimed.

The Office Action contends that column 2, line 56 to column 4, line 68 teaches that if a fraction occurs in the signal lines

of the plurality of columns, the number of output terminals of one of the plurality of driver circuits is set to the fraction. However, a review of this passage further highlights that this teaching is not found within Takaeda.

Because all features are not found within Takaeda, this reference fails to anticipate claim 1 and the claims dependent thereon.

The features of claim 9 have been wholly incorporated into claim 3 to for amended claim 3. Thus, previous claim 9 is now amended claim 3. Within amended claim 3:

> the number of output terminals of each of said plurality of driver circuits is set to a same number,
>
> when a size of a frame portion adjacent to said display portion is specified, the number (n) of output terminals of each of said plurality of driver circuits is determined on the basis of said specified frame size by the number of lines which can be wired into a wiring region of said frame portion,
>
> when the total number of signal lines of said plurality of

columns which is decided by a display system is set to N, the number of said driver circuits is set to N/n.

The Office Action contends that Takaeda teaches the number (n) of output terminals of each of said plurality of driver circuits = 3.

The Office Action further contends that Takaeda teaches the total number of signal lines of the plurality of columns which is decided by a display system is set to N.

In response, figure 2 of Takaeda arguably teaches a plurality of signal lines 11-b (column 2, line 63) and a driver circuit 13. But Takaeda fails to teach total number of signal lines as set to N. Instead, and indeterminate amount of signal lines 11-b are present within Takaeda.

Even still, note that ***only one*** drive circuit 13 is shown within Takaeda (see figure 2). Thus, the ratio N/n within Takaeda must be 1 within Takaeda, since only one drive circuit 13 is present within Takaeda. But the Office Action contends that n equals 3. Using this logic provided within the Office Action, total number of signal lines "N" must also equal 3 since ratio N/n within Takaeda must be 1 as shown hereinabove. However, note

that figure 2 of Takaeda depicts more than 3 signal lines 11-b for each drive circuit 13. As a result, the teachings of Takaeda fail to achieve the claimed invention, especially in light of the above-provided example.

Within claim 25 and the claims dependent thereon, each driver circuit of said plurality of driver circuits having a plurality of output terminals, said plurality of output terminals providing a plurality of signal potentials to a group of signal lines of said plurality of signal lines, said group of signal lines being less than all of said plurality of signal lines.

The Office Action contends that column electrodes 11-b of Takaeda (column 2, line 63) are the claimed signal lines. The Office Action further contends that $q_1$ to $q_N$ of Takaeda (figures 1(A), 2, 3) are the claimed drive circuits. In this regard, $q_1$ to $q_N$ and $Q_1$ to $Q_N$ are both shown within Takaeda. While $q_1$ to $q_N$ is within the drive circuit 13 and is connected to gate circuit 37, $Q_1$ to $Q_N$ of Takaeda are arguably connected to column electrodes 11-b (column 5, lines 4-5). Thus, it is believed that buffers 36 of Takaeda, having outputs $Q_1$ to $Q_N$, are intended to be the claimed drive circuits within the Office Action.

Within the claims, each driver circuit of said plurality of

driver circuits having a plurality of output terminals. Takaeda fails to show each buffer 36 as having a plurality of output terminals. While Takaeda depicts $q_1$ to $q_N$, Takaeda fails to teach, for example, $q_1$ as a plurality of signal potentials to a group of signal lines of said plurality of signal lines. Instead, $q_1$ is connected to only one signal line 11-b.

Withdrawal of this rejection and allowance of the claims is respectfully requested.

Claims 13-16 were rejected under 35 U.S.C. 102 as allegedly being anticipated by U.S. Patent 5,936,617 issued to Uchino et al. (Uchino).

This rejection is respectfully traversed for at least the following reasons.

Claims 13-16 are dependent upon independent claim 3. The features of claim 9 have been wholly incorporated into claim 3 to for amended claim 3. Thus, previous claim 9 is now amended claim 3.

Note that there has been no previous rejection of prior claim 9 using Uchino as the basis of this rejection. Thus, prior

claim 9, provided as amended claim 3 is deemed to be allowable over Uchino. Withdrawal of this rejection and allowance of the claims is respectfully requested.

Additionally, if the allowance of amended claim 3 is not forthcoming and a rejection of amended claim 3 is made using Uchino or another reference other than Takeda, then this rejection can be ***properly made only within a new non-final Office Action.*** See M.P.E.P. §706.07(a), 8th Edition, August 2001.

**Newly added claims**

Within claims 40-42, a fraction is defines as (S - (OP * (DC-1))), wherein "S" is the total number of said signal lines, "OP" is the total number of said output terminals for a driver circuit of said plurality of driver circuits, and "DC" is the total number of said driver circuits. Support is provided at, for example, page 13 lines 18-26.

**Conclusion**

For the foregoing reasons, all the claims now pending in the present application are allowable, and the present application is in condition for allowance. Accordingly, favorable reexamination and reconsideration of the application in light of the amendments and remarks is courteously solicited.

If the Examiner has any comments or suggestions that could place this application in even better form, the Examiner is requested to telephone Brian K. Dutton, Reg. No. 47,255, at 202-955-8753 or the undersigned attorney at the below-listed number.

Respectfully submitted,

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